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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,840	11/21/2001	Peter Irma August Barri	RAL920000112US2	3016

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	8

DATE MAILED: 12/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,840	BARRI ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed October 13, 2003 in response to PTO Office Action dated September 30, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-28 have been presented for examination in this application. In response to the last Office Action, claims 10-22 have been canceled. Claims 1-9 and 23-28 have been elected.

The Examiner has considered the arguments regarding the election of Group I and Group III, and has withdrawn the requirement for restriction with regards to claims 23 and 24. Consequently, the claims of Group III (23 & 24) have been re-adjoined with the claims of Group I (1-9 and 25-28) and an action based on the these claims will be given by the Examiner.

Claim Objections

Claims 1, 2, 4-7, 23-25 and 27 are objected to because of the following informalities:

Regarding claim 1:

Insert –different-- before "memories" in lines 5, 7, 13, and 14.

Insert –of the N different memories-- after the second instance of "memory" in line 8.

Replace "memory set" in line 12 with –different memories— in order to facilitate proper antecedent basis.

Insert –M different— before "busses" in line 13.

Insert –of the M different busses— after "bus" in line 14.

Regarding claim 2:

Insert –different-- before "memories" in line 1.

Regarding claim 4:

Insert –is— after "spread" in line 2.

Regarding claims 5 and 6:

Replace "buffer is" in line 1 with –of the at least one buffers are— in order to facilitate proper antecedent basis.

Regarding claim 7:

Insert –at least one— before "buffer" in line 2.

Regarding claim 23:

Replace "is" in line 2 with –are--.

Please insert –a— after "communication" in line 3 since this is the first instance a "communication device" has been claimed.

Regarding claim 24:

Replace "one of the memory elements" with –of said ones of the plurality of separate memory elements— in order to facilitate relating the busses with the specific separate memory elements.

Regarding claim 25:

Replace "said memories" in line 5 with –said selected ones of said plurality of separate memories— in order to coincide with the previously recited claimed elements.

Regarding claim 27:

Insert –of the multiple— after "parts" in line 5 in order to coincide with the previously recited claim limitations.

Replace the second instance of "the" in line 5 with "said separate" in order to coincide with the previously recited claim limitations.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9, 23, 24, and 26-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "M different busses...operatively coupled to one of the N memories" in lines 4-5. It is unclear from the claim language whether all of the "M different busses are coupled to the same memory, or whether the M different busses are respectively distributed among the N memories.

Claim 9 recites the limitations "re-fresh-cycle", "DRAM controller", "R requests", "Transmitter controller", R-accesses", "corresponding EPC queue[Slice; QW], "EPC", "globally W excluded slices", "slice exclusion rules", "Receiver", "W requests", "non-excluded slices", "last assigned slice", "Receiver Controller", "previous window", "W-access", "EPC accesses", EPC queue [Slice; QW]", "EPC requests", and "Weight". There is insufficient antecedent basis for these limitations in the claim. It is unclear to the Examiner how these limitations correspond to the claimed invention of parent claim 1.

Claim 23 recites the limitation "the frame" in line 4. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner whether "the frame" relates to the "frames" of line 2.

Claim 23 recites the limitation "different memory elements" in line 4. It is unclear to the Examiner whether the "different memory elements" relate to the "separate memory elements" of line 2.

Claim 24 recites the limitation "the two parts" in line 3. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner whether "the two parts" relates to the "at least two parts" of claim 23.

Claim 24 recites the limitation "the memories" in line 2. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner whether "the memories" relates to the "a plurality of separate memory elements" of claim 23.

Claim 26 recites the limitation "activated busses" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 26 and parent claim 25 failed to recite such "activated busses", and it is unclear to the Examiner whether the "individual busses" constitute some/all/none of the "activated busses".

Claim 27 recites the limitation "multiple memory modules" in lines 7 and 9. There is insufficient antecedent basis for this limitation in the claim. The limitation "multiple memory modules" had not been previously recited, and it is unclear to the Examiner whether the "multiple memory modules" relate to the "separate memory modules" of line 2, the "different ones of the memory modules" of lines 5-6, or other memory modules.

Claim 27 recites the limitation "a communication device" in line 10. It is unclear to the Examiner whether the "a communication device" of line 10 corresponds to one of the "communication devices" of line 3, or whether the "a communication device" of line 10 is directed toward another, separate communication device.

Claim 28 recites the limitation "the controller" in line 1. There is insufficient antecedent basis for this limitation in the claim. Parent claim 1 recites "a plurality of memory controllers" in line 6, but does not mention a single memory controller like that found in claim 28.

Claims 2-8 are rejected as being dependent upon a previously rejected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

The prior art rejections have been made in light of the 35 USC 112, second paragraph rejections to the claims.

Claims 1-4, 25, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Bass et al. (US# 6,460,120)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(memory controllers)** are coupled to the multiple different memories. The arbiters control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18). The **access vector** as claimed refers to the logical address translation for data from the memory that must inherently occur due to the logical division of the memories and the associated logical simultaneous access. Although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al.

teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses. Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple buses at the same time. Thus, **total bandwidth of all of the separate busses** related to the simultaneous read access is inherently **greater than the bandwidth of an individual bus** in the Bass et al. invention.

Regarding claim 2, Bass et al. teaches that the first mode may be a **read mode**, which is a sub-section of the TDM-mode in the form of read-only (col. 24, lines 59-63).

Regarding claim 3, Bass et al. teaches that the memory options may include multi-bank **DDR DRAM** (col. 9, lines 46-48).

Regarding claim 4, Bass et al. teaches partitioning the memory into at least **four banks with a buffer spread across the four banks** (col. 9, lines 55-60).

Regarding claim 25, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(memory controllers)** are coupled to the multiple different memories. The arbiters control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that

these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18).

Regarding claim 26, although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses. Since Bass et al. also teaches that multiple memories may be read from simultaneously, the multiple pieces of data will be read over the multiple buses at the same time. Thus, **total bandwidth of all of the separate busses** related to the simultaneous read access is inherently **greater than the bandwidth of an individual bus** in the Bass et al. invention.

Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by Bartoldus et al. (US# 6,560,227).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 23, Bartoldus et al., teaches a chip (controller) for **partitioning a frame** into **at least two parts (segments)**, where the segments are stored in N sets of 74 byte ping pong buffers (**plurality of memory elements)** (col. 2, lines 12-20). The segments are (**adjoining**) parts of the same frame, where the frame is sent over various LAN switches (**communication device**) and routing devices (col. 2, lines 1-11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 24 is rejected under 35 U.S.C. 103(a) as being obvious over Bartoldus et al. (US# 6,560,227) in view of Bass et al. (US# 6,460,120).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and

reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

The prior art rejections have been made in light of the 35 USC 112, second paragraph rejections to the claims.

Bartoldus et al., teaches a chip (controller) for **partitioning a frame** into **at least two parts (segments)**, where the segments are stored in N sets of 74 byte ping pong buffers (**plurality of memory elements)** (col. 2, lines 12-20). The segments are (**adjoining**) parts of the same frame, where the frame is sent over various LAN switches (**communication device**) and routing devices (col. 2, lines 1-11).

The difference between the claimed subject matter and that of Bartoldus et al., disclosed supra, is that claim 24 recites that an arbiter, in response to a request, causes data (parts) to be read simultaneously from the memory elements over separate busses.

Regarding claim 24, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(memory**

controllers) are coupled to the multiple different memories. The arbiters control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Bartoldus et al. and Bass et al. before him at the time the invention was made to modify the network system of Bartoldus et al. to include the simultaneous access memories of Bass et al., because then the requested data could be retrieved from the memories in a quicker fashion and use less processing cycles.

Claim 27 is rejected under 35 U.S.C. 103(a) as being obvious over Bartoldus et al. (US# 6,560,227) in view of Bass et al. (US# 6,460,120) and Applicant's Admitted Prior Art (AAPA).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an

invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

The prior art rejections have been made in light of the 35 USC 112, second paragraph rejections to the claims.

Bartoldus et al., teaches a chip (controller) for **partitioning a frame** into **at least two parts (segments)**, where the segments are stored in N sets of 74 byte ping pong buffers (**plurality of memory elements)** (col. 2, lines 12-20). The segments are (**adjoining**) parts of the same frame, where the frame is sent over various LAN switches (**communication device**) and routing devices (col. 2, lines 1-11).

The difference between the claimed subject matter and that of Bartoldus et al., disclosed supra, is that claim 27 recites simultaneously reading data from multiple memories where the total bandwidth output from the memories matches the bandwidth of a FAT pipe port on a communication device.

Regarding claim 27, Bass et al. teaches, as seen in Figure 13, **multiple (N) different memories** such as DRAM memories. Each of these memories is attached to an associated one of the multiple **(M) different buses**, which inherently facilitate data movement according to a certain bandwidth. A plurality of arbiters **(memory controllers)** are coupled to the multiple different memories. The arbiters control the accessing of the memories, as well as the modes for accessing the memories. The memories can be **set into two modes of operation** (col. 24, lines 36-63). Bass et al. further teaches that the memories are logically divided into sub-memories, and that these sub-memories can be logically **accessed simultaneously**. The arbiter of Bass et al. allows for such accesses in the form of writes or **read accesses** (col. 25, lines 10-18), where the read accesses are part of a read **window**. Although the Bass et al. reference does not specifically recite bandwidth in terms of the busses and memories, Bass et al. teaches that data can be read from the memories, which would inherently mean that the data travels at some speed relative to the bandwidth of the busses.

AAPA teaches that **FAT pipes** are high bandwidth channels for transmitting large amounts of data, and can be included in high-speed storage subsystems (page 2, lines 6-10).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Bartoldus et al., Bass et al., and AAPA before him at the time the invention was made to modify the network system of Bartoldus et al. to include the simultaneous access memories of Bass et al. and FAT pipe bandwidth of AAPA, because then the

requested data could be retrieved from the memories in a quicker fashion and use less processing cycles according to the simultaneous access and FAT pipe features.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

DS/BRP

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

November 28, 2003